

Notice of References Cited	Application/Control No. 10/801,828	Applicant(s)/Patent Under Reexamination LAI ET AL.	
	Examiner Theresa T. Doan	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,311,040 A	05-1994	Hiramatsu et al.	257/57
	B	US-6,423,578 B2	07-2002	Maeda, Tatsuro	438/118
	C	US-6,639,246 B2	10-2003	Honda, Tatsuya	257/72
	D	US-			
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	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Denton et al. ("Fully Depleted Dual-Gated Thin-Film SOI P-MOSFET's fabricated in SOI Islands with an Isolated Buried Polysilicon Backgate", IEEE Electron Device Letters, Vol. 17, No. 11, November 1996, pgs. 509-511).
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.